

**Date:** February 15th

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**To:** Dr. Kaputa

**Subject:** Lab 2 – PWM Module

Introduction

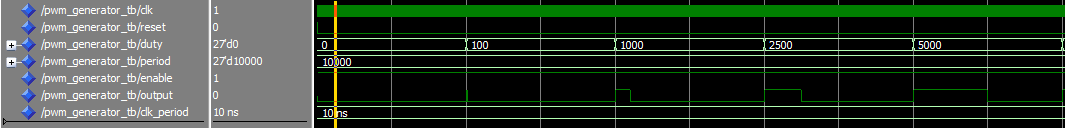
The PWM module is built upon the baseline *blink* module provided in class. To fulfill the requirements and for flexibility, the PWM module has an enable input port, an input port for period, and an input port for duty cycle. The period and duty input ports are 27-bit vectors so signal with period up to 1 second can be generated. The input clock frequency is assumed to be 100 MHz.

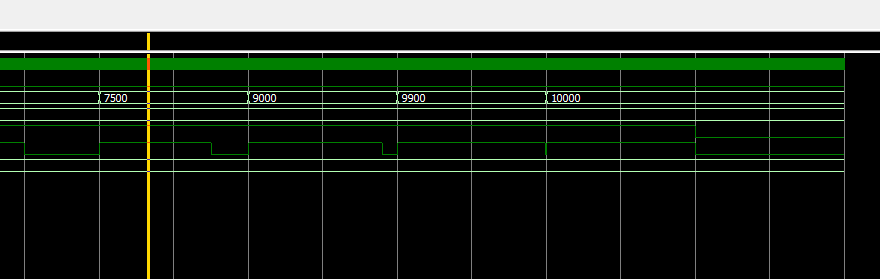
The reason for this analysis is that the duty and period of the output signal should be able to be modified in real time with any valid values (within 27 bits). The output signal should then show the correct period and duty cycle. The PWM module should also be turned off anytime with the enable port.

The below analysis verifies PWM operation in all corner cases. Duty cycle is changed overtime to demonstrate the module’s ability to reflect the change on the output.

Analysis

A test bench was used to verify functionality. A period of 1 KHz was used. The test is conducted through Modelsim using a test bench.





Conclusion

The PWM module is proven to be able to generate immediate output according to the input ports’ values. The maximum value that can be used for input ports is 227. In addition, users have to calculate their desired period based on the input clock frequency.